REMARKS

This is a Response to the currently pending Office Action that was mailed on January 19, 2007. The Office Action objected to the present application based on an alleged failing to provide proper antecedent basis for the claimed subject matter and rejected claims 63-77 and 80-124 under 35 U.S.C. 112, second paragraph, on the corresponding grounds. It is respectfully submitted that not only are these objections and rejections are incorrect, but that they are further improper.

All of these specific grounds have been brought up in previous Office Actions (mainly as rejections under 112, first paragraph, written description) and withdrawn based on the corresponding responses. The Office Action is improperly bringing them up here again under the guise of objections to the specification and under 35 U.S.C. 112, second paragraph.

More specifically, with respect to claims 63-77 and 80-93, the Office Action states:

> applicant fails to provide adequate written description for channels of multi-level memory cells of a first group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a first bit line and a reference potential, channels of multi-level memory cells of a second group of the plurality of non-volatile multi-level memory cells being coupled in parallel between a second bit line and the reference potential

where the underlining is original to the Office Action. With respect to claims 63-77 and 80-93, the Office Action further states:

> applicant fails to provide adequate written description for the first, second, third, fourth verifying reference parameters (electrical values), the first, second, third reading reference parameters (electrical values), wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying reference parameter is allocated above the third reading reference parameter.

And with respect to claims 94-124, the Office Action states:

> applicant fails to provide adequate written description of parameter generating circuitry generating a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter, wherein the first read reference parameter is allocated between a level corresponding to the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter..

All three of these grounds have been raised before in the Office Action mailed on December 31, 2003, and the two last have also been raised in the Office Action mailed on May 12, 2004. Responses to these two Office Actions were respectively mailed on March 26, 2004, and August 12, 2004. The rejections where withdrawn and not present in the many subsequent Office Actions. Consequently, **the present Office Action is improperly reintroducing the present objections and rejections, which therefore must be withdrawn.**

For the convenience of the Examiner, the previously presented arguments are represented here. The following comments were given in the Response (March 26, 2004) to the Office Action mailed on December 31, 2003:

Support for Claims 63-77 and 80-106

Applicants have previously supplied support for all of the pending claims in the Amendment of September 9, 2003, submitted in response to the previous Office Action. This previous Amendment provided support in a two-column format; although the Applicants believe that the previous Amendment presented sufficient support, the present Amendment provides further detail for those specific elements where the Office Action feels more explanation is required.

More specifically, the Office Action states: "For example, for claim 63, Applicant must point out where in the specification the channels of multi-level cells are being coupled between the bit line and the reference potential, or what are the verifying reference parameters and the reading reference parameters are. Applicant directed to Figures 11c, 11d, 15a, 15b of Patent '344, but did not specifically point out each element or limitation."

For "channels of multi-level cells are being coupled between the bit line and the reference potential":

The cells shown as T_{10}, T_{11}, etc. in Figure 15a of `344 and 500a, 500b, etc. in Figure 15b of `344. In Figure 15a, these are connected between ground (a reference potential) and the bit lines connected to V_{D0}, V_{D1}, etc. Figure 15b is a virtual ground array with the cells connected between two bit lines, the connection to the reference potential being through one of the bit lines, where the values are given in Figure 17b. The Office Action is correct in that these figures do not explicitly show the channel. The channel region is explicitly shown in the many schematic figures of cells shown in the

earlier figures of `344; for example, see Figure 5a where the channel of cell 500a is indicated by reference numbers 520a and 512a.

Also see Figure 12 of the present application, which shows cells 63, 65, ..., again connected in a virtual ground array between bit lines 91, 93, ..., through which the cell is connected on one side to a reference potential whose values are given in Figures 26 and 27. The channel is shown explicitly in Figure 9, where it is indicated by L1 and L2.

For the "verifying reference parameters":

These are shown in Figure 11c of the `344 patent (which is also Figure 15B of the present application). These are the reference current $I_{REF("3")}$, $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-50, of `344, where the emphasis is added:

> ... For a four state storage, four sense amplifiers, each with its own distinct current reference levels IREF,0, IREF,1, IREF,2, and IREF,3 are attached to each decoded output of the bit line. ... .
>
> *During programming*, the four data inputs Ii (I0, I1, I2 and I3) are presented to a comparator circuit which also has presented to it the four sense amp outputs for the accessed cell. If Di match Ii, then the cell is in the correct state and no programming is required. If however all four Di do not match all four Ii, then the comparator output activates a programming control circuit. This circuit in turn controls the bit line (VPBL) and word line (VPWL) programming pulse generators. A single short programming pulse is applied to both the selected word line and the selected bit line. This is followed by a second read cycle to determine if a match between Di and Ii has been established. This sequence is repeated through multiple programming/reading pulses and is stopped only when a match is established (or earlier if no match has been established but after a preset maximum number of pulses has been reached).
>
> The result of such multistate programming algorithim is that each cell is programmed into any one of the four conduction states in direct correlation with the reference conduction states I_{REF}, i. ...

For the "reading reference parameters":

These are also shown in Figure 11c of the `344 patent (which is also Figure 15B of the present application). These are again the reference current $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-18, of `344, except that for the embodiment to which the present claims are drawn, for the read process these are shifted with respect to their values as programming reference parameters so that they are

arranged as described in the claim. This is described at 26, lines 51-65, of `344, where the emphasis is added:

> In actual fact, although four reference levels and four sense amplifiers are used to program the cell into one of four distinct conduction states, only three sense amplifiers and three reference levels are required to sense the correct one of four stored states. For example, in FIG. 11c, I sub REF ("2") can differentiate correctly between conduction states "3" and "2", I sub REF ("1") can differentiate correctly between conduction states "2" and "1", and I sub REF ("0") can differentiate correctly between conduction states "1" and "0". *In a practical implementation of the circuit of FIG. 11e the reference levels I sub REF, i (i=0,1,2) may be somewhat shifted by a fixed amount during sensing to place them closer to the midpoint between the corresponding lower and higher conduction states of the cell being sensed.*

Consequently, the three reading reference parameters are placed between the four programming parameters as described in the manner described in the claims.

Rejections under 35 U.S.C. 112, first paragraph

The Office Action has rejected claims 63-77, 80-93, and 94-124 all under 35 U.S.C. 112, first paragraph, due to lack of support for the verifying reference parameters and for these parameters not being related to the reading reference parameters as described in the claims. This has been addressed in the preceding section, where support for these elements is given.

Claims 94-124 are also rejected under 35 U.S.C. 112, first paragraph, as failing to provide an adequate written description for the parameter generating circuitry. In a particular embodiment of the present invention, these parameters are various reference currents that are provided by reference cells. In various embodiments, these reference cells are shown as 431, 433, 435 in Figure 17B; as MASTER REF. CELLS 507 in Figure 18; in Figure 20A as 523, 525, 529; in Figure 21A as 523, 525, 531; in Figure 21 as 551, 553, 555; and in Figure 21C. These circuits are described in detail in the section of the material included by the Preliminary Amendment filed concurrently with the present application entitled "Read Circuits and Techniques Using Reference Cells" which begins on page 9, line 19, of the Preliminary Amendment.

The following comments were given in the Response (August 12, 2004) to the Office Action mailed on May 12, 2004, where references to an Attachment A refer to the attachment that accompanied the response of August 12, 2004:

Rejections under 35 U.S.C. 112, 1st ¶: Verifying and Reading Reference Parameters

The Office Action has rejected claims 63-77 and 80-124 under 35 U.S.C. 112, first paragraph, due to lack of support for the verifying reference parameters and for these parameters not being related to the reading reference parameters as described in the claims. This rejection is respectfully submitted to be in error. As these parameters are all similarly described in the various claims, reference will be made to claim 63, with the support for the other claims following in a similar manner. With respect to the support provided below, it is again noted that the present application presents a number of embodiment and the following support is based on only one example of these.

The Examiner's attention is directed to Attachment A, which accompanies the present Response and to which reference is made in the following.

In particular, the elements for which the Office Action fails to find support are listed below for the case of claim 63. The corresponding support is then provided for each of these with reference to the Figure 11c of the `344 patent (which is also Figure 15B of the present application), Figure 11e of the `344 patent, and the description of these figures at column 34, line 5, to column 26, line 65, of the `344 patent. Attention is particularly called to lines 4-65 of column 26.

More specifically, the verifying reference parameters are described in claim 63 as:

> verifying whether the parameter of the one non-volatile multi-level memory cell has being settled to the one state selected from the plurality of states by comparing the parameter of the one non-volatile multi-level memory cell with a plurality of verifying reference parameters including at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter, and of repeating the operation for settling the parameter and the operation for verifying until it is verified by the operation for verifying that the parameter of the one non-volatile multi-level memory cell has being settled to the one state,

Support in the present application is given in Figure 11c of the `344 patent (which is also Figure 15B of the present application). These are the reference current $I_{REF("3")}$, $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-50, of `344, where the emphasis is added:

> ... For a four state storage, four sense amplifiers, each with its own distinct current reference levels IREF,0, IREF,1, IREF,2, and IREF,3 are attached to each decoded output of the bit line. ... .
>
> *During programming*, the four data inputs Ii (I0, I1, I2 and I3) are presented to a comparator circuit which also has presented to it the four sense amp outputs for the accessed cell. If Di match Ii, then the cell is in the correct state and no programming is required. If however all four Di do not match all four Ii, then the comparator output activates a programming control circuit. This circuit in turn controls the bit line (VPBL) and word line (VPWL) programming pulse generators. A single short programming pulse is applied to both the selected word line and the selected bit line. This is followed by a second read cycle to determine if a match between Di and Ii has been established. This sequence is repeated through multiple programming/reading pulses and is stopped only when a match is established (or earlier if no match has been established but after a preset maximum number of pulses has been reached).
>
> The result of such multistate programming algorithim is that each cell is programmed into any one of the four conduction states in direct correlation with the reference conduction states I_{REF}, i. ...

Thus, it can be seen that IREF,0, IREF,1, IREF,2, and IREF,3 correspond to the "at least a first verifying reference parameter, a second verifying reference parameter, a third verifying reference parameter and a fourth verifying reference parameter" of the claim.

The reading parameters are described in claim 63 as:

> reading status of the one non-volatile multi-level memory cell by comparing the parameter with a plurality of reading reference parameters including at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter,

These are also shown in Figure 11c of the `344 patent (which is also Figure 15B of the present application). These are again the reference current $I_{REF("2")}$, $I_{REF("1")}$, and $I_{REF("0")}$, which are used as is described at column 26, lines 4-18, of `344, except that for the embodiment to which the present claims are drawn, **for the read process these are shifted with respect to their values as programming reference parameters** so that they are arranged as described in the claim. This is described at 26, lines 51-65, of `344, where the emphasis is added:

> ... only three sense amplifiers and three reference levels are required to sense the correct one of four stored states. For example, in FIG. 11c, I sub REF ("2") can differentiate correctly between conduction states "3" and "2", I sub REF ("1") can differentiate correctly between conduction states "2" and "1", and I sub REF ("0") can differentiate correctly between conduction states "1" and "0". *In a practical implementation of the circuit of FIG. 11e the reference levels I sub REF, i (i=0,1,2) may be somewhat shifted by a fixed amount during sensing to*

> *place them closer to the midpoint between the corresponding lower and higher conduction states of the cell being sensed.*

Consequently, it can be seen that the ***shifted*** values of IREF,0, IREF,1, and IREF,2 used during sensing correspond to the "at least a first reading reference parameter, a second reading reference parameter and a third reading reference parameter" of the claim.

The relation of the reading parameters to the states is described in claim 63 as:

> wherein the first reading reference parameter is allocated between the first state and the second state, the second reading reference parameter is allocated between the second state and the third state, and the third reading reference parameter is allocated between the third state and the fourth state,

This is illustrated in Figure A of the Attachment A, where the first read parameter is labeled as Read 1, the first state is labeled as State 1, and so on for the other read parameters and states. As described in the italicized portion of at the end of the portion of the specification quoted in the last paragraph, the *shifted* values of IREF,0, IREF,1, and IREF,2 are arranged with respect to the states of cell as shown in Figure C. Figure C corresponds to Figure 11c of `344 along the dotted line at V_{CG}=5.0, for example. It can be seen that Figure A and Figure C describe the same relations, with the following identifications: State 1~"0"; State 2~"1"; State 3~"2"; State 4~"3"; and Read 3~I_{REF} ("2"), sense; Read 2~I_{REF} ("1"), sense; Read 1~I_{REF} ("0"), sense.

The reading parameters are described further in claim 63 as:

> wherein the first reading reference parameter, the second reading reference parameter and the third reading reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile multi-level memory cell can be read out by output data of a plurality of bits,

This is just stating that each "reading reference parameter" is used for normal sensing of the state of a multi-state memory cell, as is described, for example, at column 24, lines 5-38, of the application and which is developed more fully over the next two and a half columns.

The relation of the reading parameters to verifying reference parameters is described in claim 63 as:

> wherein the first verifying reference parameter is allocated below the first reading reference parameter, the second verifying reference parameter is allocated between the first reading reference parameter and the second reading reference parameter, the third verifying reference parameter is allocated between the second reading reference parameter and the third reading reference parameter and the fourth verifying

> reference parameter is allocated above the third reading reference parameter.

This is illustrated in Figure B of the Attachment A, where the first verify parameter is labeled as Verify 1 and so on for the other verify parameters. This is described at 26, lines 51-65, of `344, where the emphasis is added:

> In actual fact, although four reference levels and four sense amplifiers are used to program the cell into one of four distinct conduction states, only three sense amplifiers and three reference levels are required to sense the correct one of four stored states. For example, in FIG. 11c, I sub REF ("2") can differentiate correctly between conduction states "3" and "2", I sub REF ("1") can differentiate correctly between conduction states "2" and "1", and I sub REF ("0") can differentiate correctly between conduction states "1" and "0". *In a practical implementation of the circuit of FIG. 11e the reference levels I sub REF, i (i=0,1,2) may be somewhat shifted by a fixed amount during sensing to place them closer to the midpoint between the corresponding lower and higher conduction states of the cell being sensed.*

Consequently, the *shifted* values of IREF,0, IREF,1, and IREF,2 used as reading reference parameters are arranged with respect to the programming reference parameters IREF,0, IREF,1, IREF,2, and IREF,3 as shown in Figure D. (Figure D would again corresponds to Figure 11c of `344 along the dotted line at V_{CG}=5.0, for example.) It can be seen that Figure A and Figure C describe the same relations, with the following identifications: Verify 4~I_{REF} ("3"), program verify; Verify 3~I_{REF} ("2"), program verify; Verify 2~I_{REF} ("1"), program verify; Verify 1~I_{REF} ("0"), program verify and Read 3~I_{REF} ("2"), sense; Read 2~I_{REF} ("1"), sense; Read 1~I_{REF} ("0"), sense.

Concerning the comments of the Office Action in its paragraph 10, the Office Action admits that column 26, lines 51-65, of the `344 describes shifting the values of I_{REF} during sensing relative to that used for program verify. However, it then goes on to state that "There is no show or suggestion of separate verifying reference parameters and reading reference parameters". This is respectfully submitted to be in error. If the parameters have different values, they are different parameters. As described above, the present application is believed to clearly support what is actually found in the claims themselves as they are written.

Consequently, it is therefore respectfully submitted that the rejections under 35 U.S.C. 112, first paragraph, due to lack of support for the verifying reference parameters and for these parameters not being related to the reading reference parameters as described in the claims are not well founded and should be withdrawn. If the above does

not address the particular concerns of the Examiner with respect to these elements, a phone call to the undersigned would be welcomed.

Rejections under 35 U.S.C. 112, 1st ¶: Parameter Generating Circuitry

Claims 94-106 are also rejected under 35 U.S.C. 112, first paragraph, as failing to provide an adequate written description for the parameter generating circuitry that is additionally included in these claims. These are shown in Figure 11e of the '344 patent as the current sources $I_{REF,0}$, $I_{REF,1}$, $I_{REF,2}$, $I_{REF,3}$ connected to the sense amps. Specific embodiments based on reference cells are shown in Figures 17A and 17B. Figure 17A shows MASTER REFERENCE CELL 1400 supplying current along line 1403 to SENSE AMPLIFIER 1410. Figure 17B shows reference cells 1431, 1433, 1435 supplying current along line 1441 to SENSE AMPLIFIER 1440. These circuits are described in detail in the section of the material included by the Preliminary Amendment filed concurrently with the present application entitled "Read Circuits and Techniques Using Reference Cells" which begins on page 9, line 19, of the Preliminary Amendment, with particular reference to page 12, line 6, to page 14, line 14.

Specifically, page 12, lines 20-28:

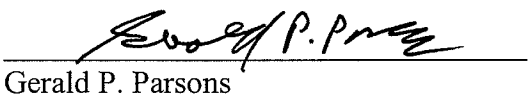
> ... Co-pending patent application, Serial No. 204,175 proposes using the same sensing amplifiers and I_{REF}'s for both programming and reading. This provides good tracking between the reference levels (broken curves in figure 15B) and the programmed levels (solid curves in figure 15B).
>
> In the improved scheme of the present invention, the I_{REF}'s are themselves provided by the source-drain currents of a set of EEprom cells existing on the same chip and set aside solely for this purpose. Thus, they act as master reference cells with their I_{REF}'s used as reference levels for the reading and programming of all other EEprom cells on the same chip.

And at page 13, lines 12-14:

> Once the reference threshold voltage V_{TI} or reference drain-source current I_{REF} is programmed into each reference cell 1400, it then serves as a reference for the reading of an addressed memory cell such as cell 1420.

As can be seen from the above-reproduced comments, the objections/rejections of the present Office Action are also incorrect. Therefore, for at least these reasons, it is respectfully submitted that the objections and rejections of the present Office Action are both incorrect and improper, and should consequently be withdrawn and the pending claims be allowed.

Respectfully submitted,



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